

QIC CARRIER BOARD

V1

USER'S MANUAL



© QUANSER CONSULTING INC., 2002

QIC

How to contact Quanser Consulting:



(905) 940-3575

Telephone



(905) 940-3576

Facsimile



80 Esna Park Drive
Markham, ON
Canada L3R 2R6

Mail



<http://www.quanser.com/qic/>

Web



<mailto://qic@quanser.com>
<mailto://support@quanser.com>
<mailto://info@quanser.com>

Information about QIC
Support for QIC
General information

User's Manual

QIC is a trademark of Quanser Consulting, Inc.

PIC, and PIC16F877 are a trademarks of Microchip Technology Inc.

Other brands and their products are trademarks or registered trademarks of their respective holders and should be noted as such.

© 2002 Quanser Consulting Inc.

All rights reserved. This work may not be translated or copied in whole or in part without the written permission of the copyright holder, except under the terms of the associated software license agreement. No part of this manual may be photocopied or reproduced in any form.

The use of general descriptive names, trade names, trademarks, etc. in this publication, even if the former are not especially identified, is not to be taken as a sign that such names as understood by the Trade Marks and Merchandise Marks Act, may accordingly be used freely by anyone.

Printed in Canada.

TABLE OF CONTENTS

1 INTRODUCTION	1
1.1 Carrier V1 Features.....	1
1.2 Carrier V1 Feature Locations.....	1
2 POWER SUPPLY	3
3 ANALOG INPUTS AND OUTPUTS	6
3.1 Analog Inputs (A/D).....	6
3.1.1 Analog Input (A/D) Signal Conditioning Details.....	7
3.1.1.1 Analog Reference Voltage (VREF).....	8
3.2 Analog Outputs (D/A)	9
3.2.1 Enabling the Low-Pass Filters.....	10
3.2.2 Analog OUTPUT (D/A) Signal Conditioning Details.....	11
4 OPTICAL ENCODER INTERFACE	12
4.1 Encoder Interface Details.....	13
4.1.1 Encoder Programming and Reading.....	15
4.1.2 Encoder Register Access.....	17
4.1.3 Encoder Programming Information.....	18
5 MEDIUM CURRENT PERIPHERAL DRIVERS	24
5.1 Peripheral Driver Configurations.....	25
5.1.1 Solenoid Driver Configuration.....	25
5.1.2 Bi-Directional DC Motor Driver Configuration.....	26
5.1.3 Stepper Motor Configuration.....	27
6 HIGH CURRENT PERIPHERAL DRIVERS	28

QIC

6.1 Installation of MOSFETS.....	31
6.2 High Current Driver Usage.....	31
6.2.1 Half Bridge (Single Ended) Usage.....	32
6.2.2 Full Bridge Usage.....	33

FIGURE INDEX

Index of Figures

Figure 1. QIC Carrier Board layout.2
Figure 2. Connecting an AC supply.3
Figure 3. Connecting a DC supply.3
Figure 4. Power supply schematic (simplified).4
Figure 5. Analog sub-section connections.6
Figure 6. Analog input (A/D) signal conditioning schematic.8
Figure 7. VREF enable jumper location details.9
Figure 8. J6 and J7 location on the carrier board.11
Figure 9. Analog output (D/A) signal conditioning schematic.11
Figure 10. Encoder interface connections.12
Figure 11. Encoder interface schematic details.14
Figure 12. Peripheral driver details.24
Figure 13. Setup of the jumpers and the location of peripheral outputs.25
Figure 14. Driving resistive and inductive loads.26
Figure 15. Connections for driving a small DC motor.27
Figure 16. Details for driving a stepper motor.27
Figure 17. Setup and connections for the high current drivers29
Figure 18. Detailed schematic of the high current drivers.30
Figure 19. Installation of the MOSFETS for the high-current drivers.32
Figure 20. Single ended output driver connection.33
Figure 21. Full bridge connection of high current output drivers.34

INDEX OF TABLES

Index of Tables

Table 1. Power supply specifications.....	5
Table 2. Input voltage to conversion value result for a 10 bit A/D.....	7
Table 3. Pin connections for the A/D inputs.....	7
Table 4. PWM output to DC voltage conversion (10 bit).....	10
Table 5. Pin connections for the D/A outputs. See for Figure 5 connection details.....	10
Table 6. X axis encoder pin names.....	13
Table 7. Y axis encoder pin names.....	13
Table 8. Interface connections from the QIC to the encoder IC.....	15
Table 9. Registers of the LS7266R1.....	17
Table 10. Peripheral driver connection details.....	24

QIC CARRIER V1 MANUAL

1 INTRODUCTION

The QIC Carrier boards offer many useful functions integrated into one convenient package. Various accessories such as the power supply, motor drivers, encoder counters and other peripherals have been combined into one board that allows rapid development of new projects. Designed to be coupled with the QIC Core Processor boards, the two units form a standard development package for robotics, control and signal conditioning applications.

1.1 CARRIER V1 FEATURES

The QIC Carrier board V1 has the following integrated features:

- On board power supply designed for use with 12VAC power, or 2 separate 12 volt batteries.
- Signal conditioning on 4 A/D channels¹.
- Signal conditioning on the PWM outputs. PWM signals can be low-pass filtered to provide clean analog output signals.
- Two quadrature encoder channels for measuring HEDS series compatible optical encoders.
- PWM Peripheral drivers rated 12V, 500mA per channel (4 channels total).
- PWM H-Bridge drivers rated 24V, 3A per channel (2 channels total).

1.2 CARRIER V1 FEATURE LOCATIONS

The following diagrams are designed to familiarize the user with the locations of the connectors on the board and the placement of the various sub-systems integrated into the carrier board.

¹ The analog signals are level shifted from the range [-5, +5] volts to [0, 5] volts and sent to the A/D pins of the QIC Processor Core.

QIC CARRIER V1 MANUAL

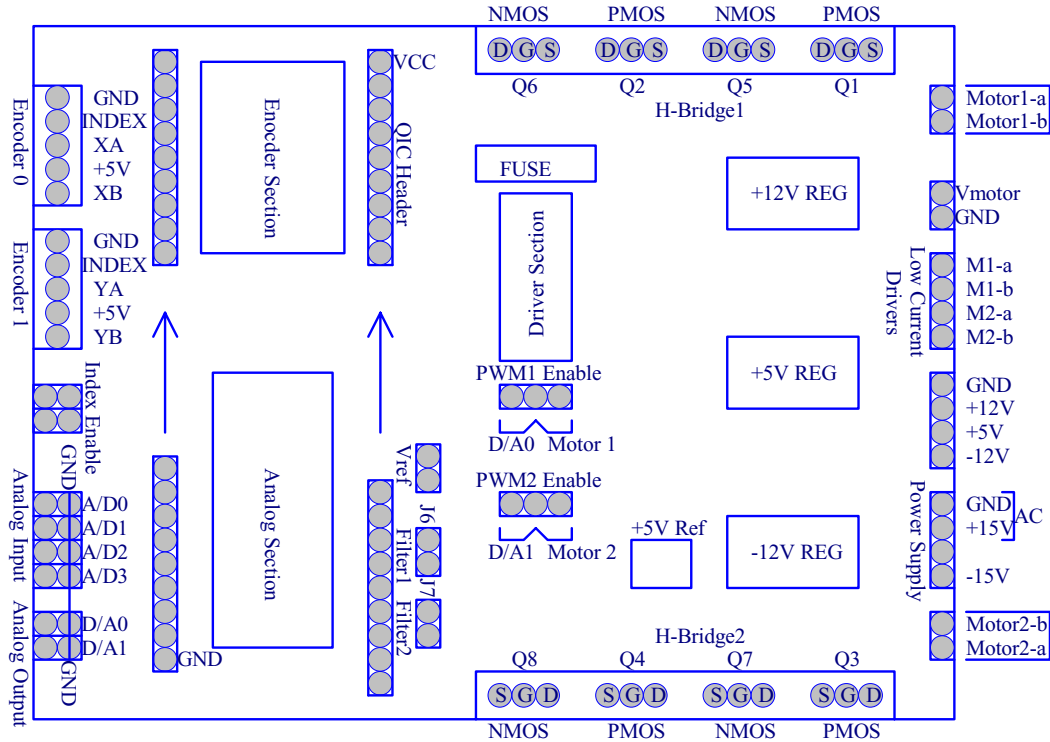


Figure 1. QIC Carrier Board layout.

The QIC Header located to the left of the board pictured in Figure 1 is designed to accept the QIC Processor Core. Note that the header connections are staggered to permit the processor core to be inserted in only one direction. Be sure that the correct orientation is noted when inserting the processor core.

When the QIC Processor Core is inserted into the carrier board, power will be provided to the core from the carrier board. There is no need for a second power supply.

QIC CARRIER V1 MANUAL

2 POWER SUPPLY

The QIC Carrier Board is designed to accept a wide range of voltage options. The board is designed to accept both an AC power supply as well as a dual (+/-) DC supply.

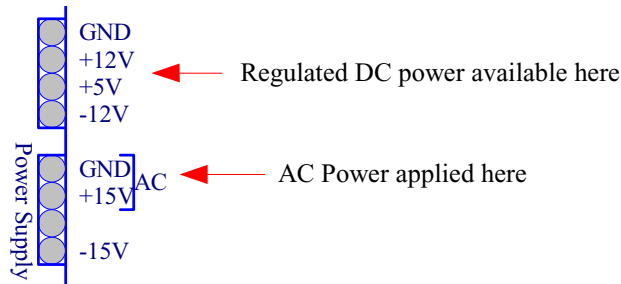


Figure 2. Connecting an AC supply.

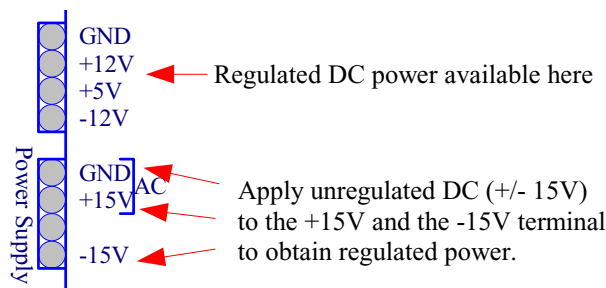


Figure 3. Connecting a DC supply.

When applying AC power to the carrier board be certain not to exceed 12VAC. Doing so may cause permanent damage to the board. AC voltage should be applied to the pins GND and +15V *only*.

Alternatively, unregulated DC power (+/- 15V) may be applied to the +15V and the -15V terminals. The ground pin (GND) should be the common point between the power supplies.

Regulated power may be applied to the regulated power connections without causing damage to the power supply circuitry. Be certain **not** to apply power to both the unregulated inputs and the regulated inputs at the same time.

QIC CARRIER V1 MANUAL

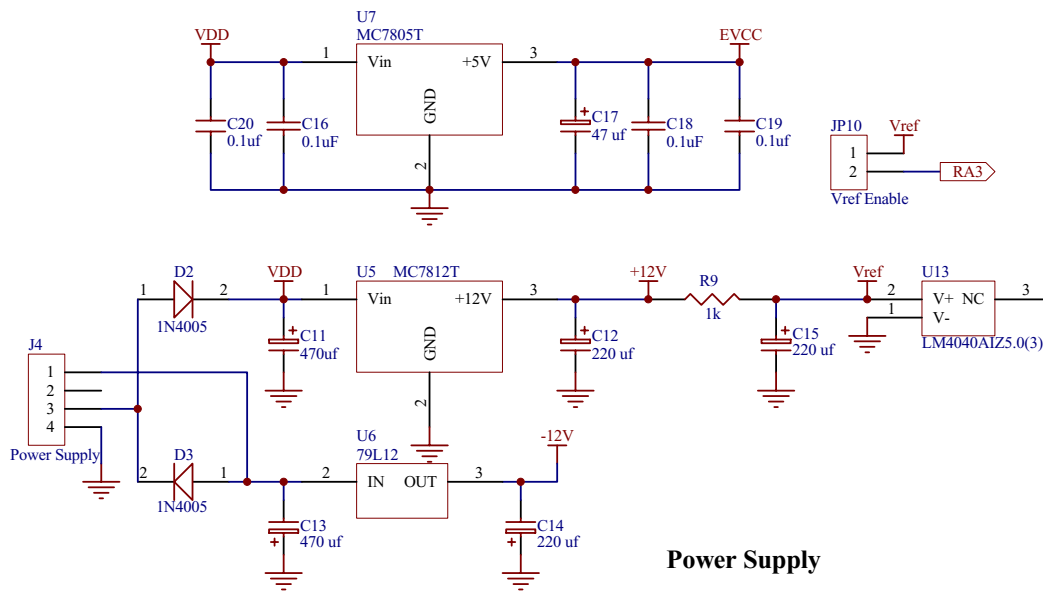


Figure 4. Power supply schematic (simplified).

QIC CARRIER V1 MANUAL

<i>Power Supply Specifications</i>		
<i>Parameter</i>	<i>Value</i>	<i>Comments</i>
Minimum AC input voltage	12VAC	Power supply must be able to provide 100mA current. ²
Maximum AC input voltage	18VAC	
Minimum DC input voltage ³	+/-15 VDC	Dual (split supplies) are required. (100mA minimum) ²
Maximum DC input voltage	+/-24VDC	The user may need to add heatsinks for continuous operation.
Maximum Current	1 Amp	Maximum of 1 amp on each of the +12V, -12V and the +5V power supplies.

Table 1. Power supply specifications.

-
- 2 Power supplies must be able to provide power for the on board circuitry, plus any additional external demands.
 - 3 Power may be provided by two 12 volt batteries, but the regulators may fail to regulate properly.

QIC CARRIER V1 MANUAL

3 ANALOG INPUTS AND OUTPUTS

The QIC Carrier Board has circuitry designed to filter both analog inputs and outputs. The analog input signal conditioning circuitry allows the user to measure a greater range of input voltages. The analog output signal conditioning circuitry filters the PWM output signals from the QIC Processor Core and makes them available as pure analog signals (high frequency component removed). For detailed information on using the PWM outputs or the A/D inputs of the PIC series of microcontrollers, please consult the Microchip web site. Additionally, the example source code included with the distribution software may be checked for examples suitable for tailoring to your application.

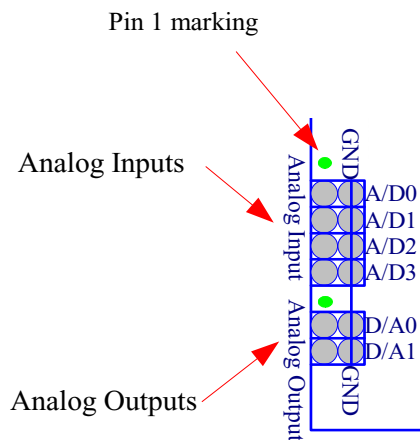


Figure 5. Analog sub-section connections.

3.1 ANALOG INPUTS (A/D)

The QIC Processor Core by itself is capable of accepting voltages in the range of 0 – 5V. To extend this range to include -5V, additional signal conditioning circuitry has been added to permit this. The conditioning performs a level shift as well as amplification to allow the 0 – 5V input to accept voltages in the range of [-5, +5] volts. Together with the 10 Bit A/D on the Processor Core, the inputs offer a complete data acquisition system.

QIC CARRIER V1 MANUAL

<i>Analog to Digital (A/D) Conversion Table</i>	
<i>Input Signal</i>	<i>A/D Conversion Register Value</i>
-5V	0
0V	511
+5V	1023

Table 2. Input voltage to conversion value result for a 10 bit A/D.

The pin connections for the signal conditioning circuitry is shown in Table 3 Note that pin 1 of the connector is indicated on the board by a square index mark.

<i>Analog Input (A/D) Pin Connections</i>			
<i>Pin</i>	<i>Signal Name</i>	<i>Pin</i>	<i>Signal Name</i>
1	A/D Channel 0	2	GND
3	A/D Channel 1	4	GND
5	A/D Channel 2	6	GND
7	A/D Channel 3	8	GND

Table 3. Pin connections for the A/D inputs.

3.1.1 ANALOG INPUT (A/D) SIGNAL CONDITIONING DETAILS

The analog input interface circuitry allows signals in the range of [-5, +5] to be applied to an A/D capable of measuring between [0, +5]. This is accomplished by subtracting an offset of V_{REF} from the signal, and then dividing the result by 2. The V_{REF} signal is obtained from the on board +5V reference. This signal is then passed on to the QIC Processor Core. The signals connect to the A/D pins of the microcontroller on board the QIC Processor Core.

QIC CARRIER V1 MANUAL

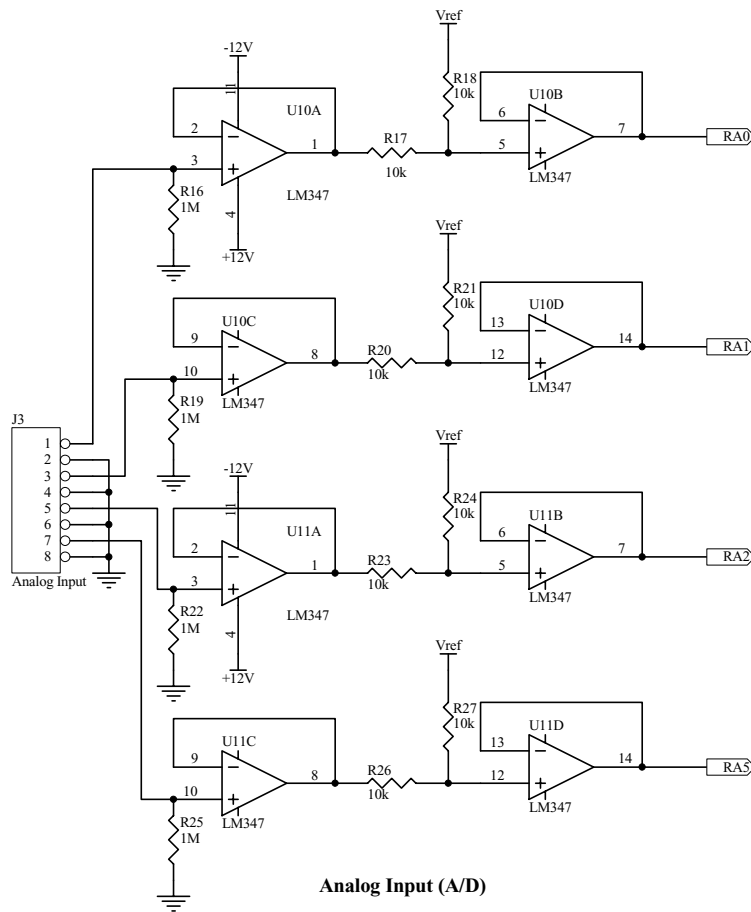


Figure 6. Analog input (A/D) signal conditioning schematic.

3.1.1.1 ANALOG REFERENCE VOLTAGE (V_{REF})

The 5 volt reference V_{REF} can also be used as the reference for the analog measurements. To enable this feature, JP10 should be installed to apply the V_{REF} signal to the A/D reference input of the QIC Processor Core. In software, the user must specify that RA3 (analog input channel 3) should be used as the reference signal for A/D measurements. Code examples are included in the distribution to show details on how to use the A/D functions.

QIC CARRIER V1 MANUAL

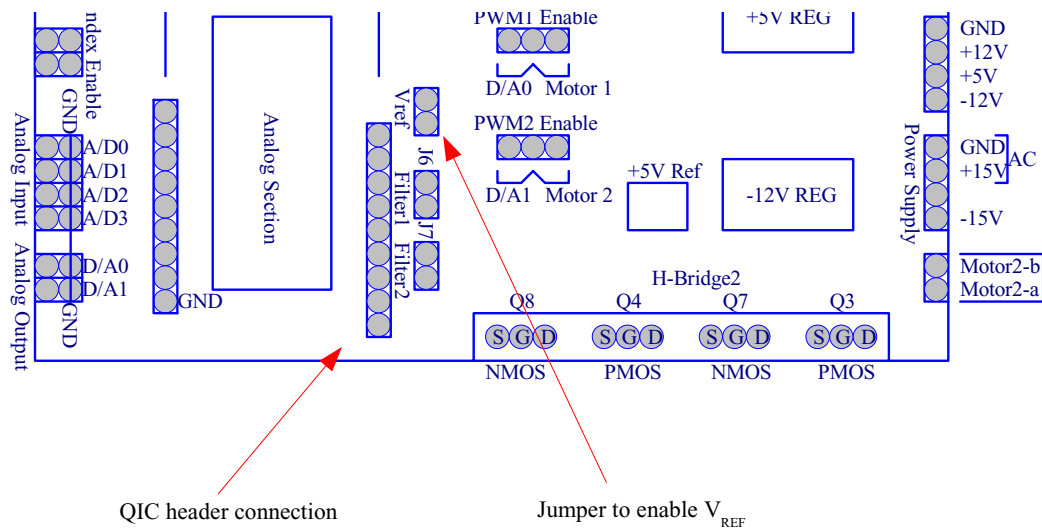


Figure 7. V_{REF} enable jumper location details.

3.2 ANALOG OUTPUTS (D/A)

The analog output interface circuitry is designed to provide analog signals from the PWM outputs of the QIC Processor Core. This is accomplished by low-pass filtering the PWM outputs. In addition, the signal is level shifted and amplified to provide a [-5, +5] output signal. Note that to enable the output on the analog channels, JP3 and JP4 must be installed in the 1-2 positions. See Figure 8 for details. The channels may be enabled independently if desired.

QIC CARRIER V1 MANUAL

<i>Digital to Analog (D/A) Conversion Table</i>		
<i>PWM Register Value</i>	<i>PWM Duty Cycle</i>	<i>DC Output Voltage</i>
0	0%	-5V
511	50%	0V
1023	100%	+5V

Table 4. PWM output to DC voltage conversion (10 bit).

<i>Analog Output (D/A) Pin Connections</i>			
<i>Pin</i>	<i>Signal Name</i>	<i>Pin</i>	<i>Signal Name</i>
1	PWM Output 0	2	GND
3	PWM Output 1	4	GND

Table 5. Pin connections for the D/A outputs. See for Figure 5 connection details.

3.2.1 ENABLING THE LOW-PASS FILTERS

The PWM output signal conditioning circuitry is fitted with low-pass filters to provide a continuous analog signal. To enable the filters, jumpers must be placed on **J6** and **J7** (refer to Figure 8). This will enable both of the low-pass filters. Alternatively, only one jumper can be installed as necessary. The filters remove the high frequency PWM signal, and pass only the lower frequency signal, thus allowing the PWM output to emulate the operation of a true switched digital to analog converter. **The low-pass filters are designed to be used with a PWM frequency of 19.5 kHz.** This should be set up in the user's software. The included code samples show details on how to do this.

QIC CARRIER V1 MANUAL

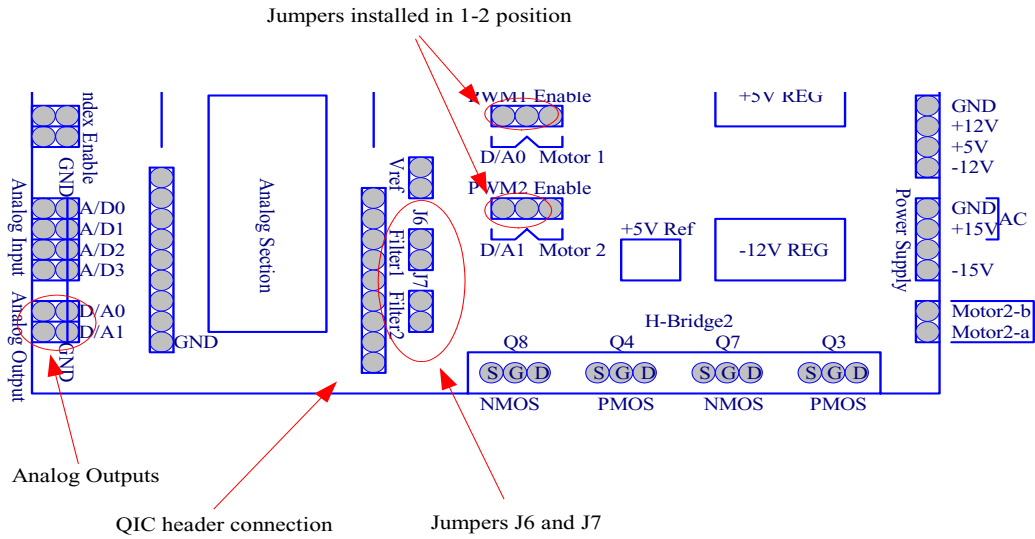


Figure 8. J6 and J7 location on the carrier board.

3.2.2 ANALOG OUTPUT (D/A) SIGNAL CONDITIONING DETAILS

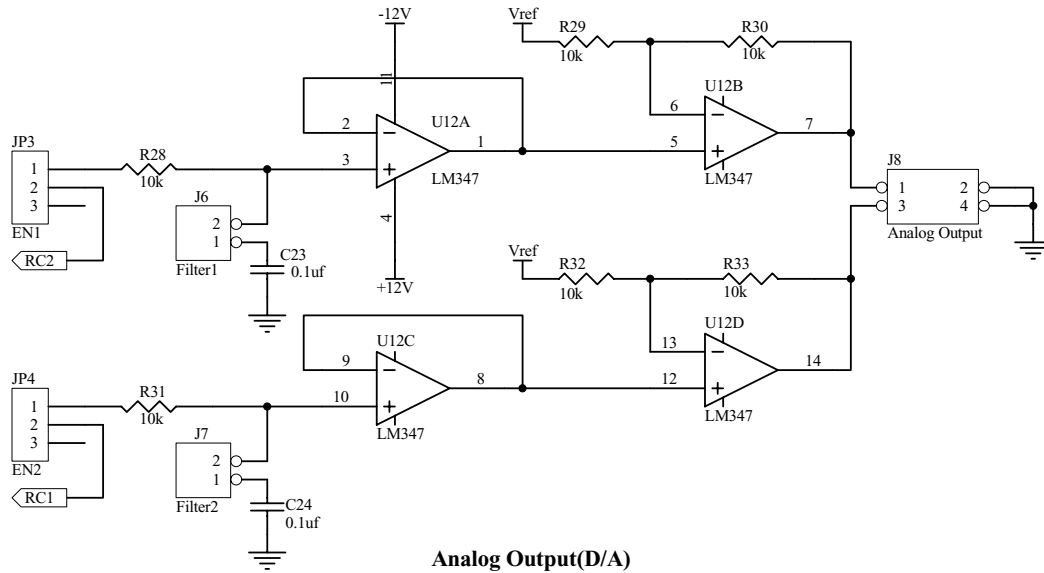


Figure 9. Analog output (D/A) signal conditioning schematic.

QIC CARRIER V1 MANUAL

4 OPTICAL ENCODER INTERFACE

The QIC Carrier board is equipped with an optical encoder interface IC. The interface IC is the LS7266R1, by US Digital (<http://www.usdigital.com>). For further details on using this IC and interfacing requirements, please see their document titled, "ls7266r1 Manufacturers' Data Sheet." Some of the information has been reprinted here for convenience.

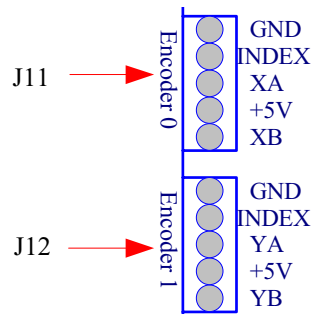


Figure 10. Encoder interface connections.

Connections to the encoders are made at connectors J11 and J12, as shown in Figure 10. Typically, the HEDS series⁴ of optical encoders are directly compatible with the encoder IC mounted on the QIC Carrier Board.

⁴ Currently, compatible encoder modules as well as parts and accessories are available from Hewlett-Packard (HP) and US Digital.

QIC CARRIER V1 MANUAL

<i>J11 - Encoder Channel 0 (X axis)</i>		
<i>Pin</i>	<i>Signal Name</i>	<i>Description</i>
1	GND	Digital ground
2	Index 0	Index signal, channel 0
3	X _A	Encoder input signal A.
4	+5V	+5V power for encoder
5	X _B	Encoder input signal B.

Table 6. X axis encoder pin names.

<i>J12 - Encoder Channel 1 (Y axis)</i>		
<i>Pin</i>	<i>Signal Name</i>	<i>Description</i>
1	GND	Digital ground
2	Index 1	Index signal, channel 1
3	Y _A	Encoder input signal A.
4	+5V	+5V power for encoder
5	Y _B	Encoder input signal B.

Table 7. Y axis encoder pin names.

Tables 6 and 7 describe the connections for the encoders. These descriptions may prove to be useful in determining if other types of encoders are compatible with the interface circuitry of the QIC system.

4.1 ENCODER INTERFACE DETAILS

Table 8, together with Figure 11, detail the connections of the encoder interface IC to the QIC Processor Core. Communicating with the encoder IC is similar to talking to a device on the bus of a processor; all data transfer is controlled via the /RD, /WR, and /CS signals. To access the device, the /CS pin must be brought low. This requires that pin RE2 of the QIC Processor Core must be in a low state. Reads or writes can then be accomplished by bringing the appropriate pin low, For a **read**, /RD or pin RE0 must be

QIC CARRIER V1 MANUAL

brought low (programmed from the QIC Processor Core). For a **write**, /WR or pin RE1 must be brought low (programmed from the QIC Processor Core). Both the read and write lines should never be simultaneously low. This may cause permanent damage to the IC, so the user should be aware of this condition. The included source code shows details on accessing the encoder IC.

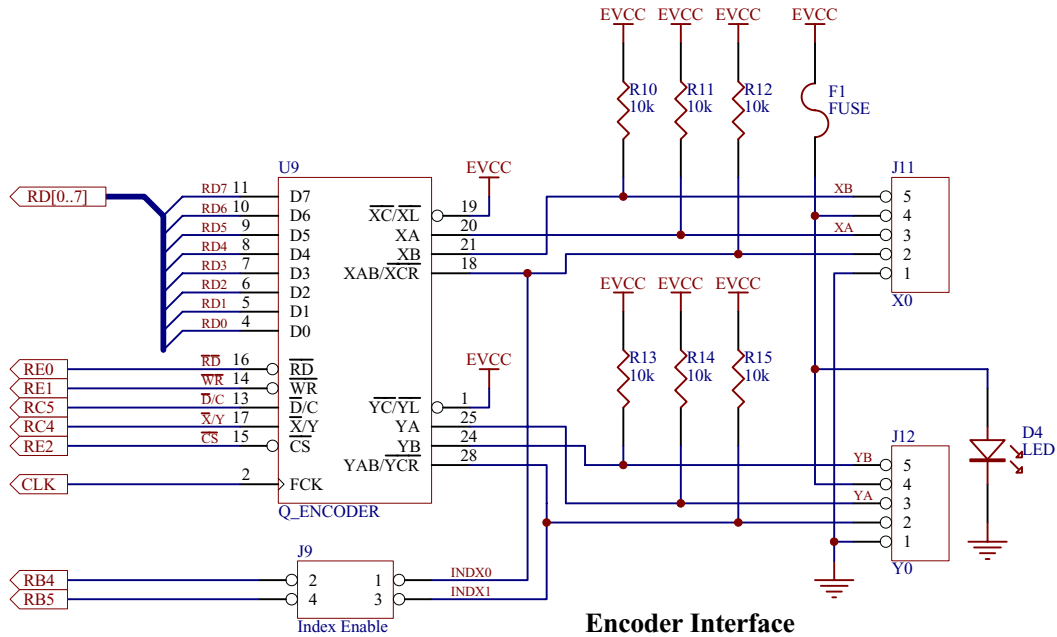


Figure 11. Encoder interface schematic details.

Table 8 Shows the connection details and the associated pins for convenience. The included source code examples show details on using the interface routines to to access the encoder and simplify programming.

QIC CARRIER V1 MANUAL

<i>Encoder Interface to QIC Processor Core Connections</i>			
<i>QIC Core</i>		<i>Encoder IC</i>	
<i>Pin</i>	<i>Signal Name</i>	<i>Signal Name</i>	<i>Description</i>
[28-35]	PORT D	Data Bus	The data bus interface to the encoder IC. This is input/out depending on the direction of data flow (/WR, /RD)
9	RE0 (/RD)	RD	Read input. At the trailing edge of a low going signal, the Flag or the Output latch registers will be transferred to the data bus.
10	RE1 (/WR)	WR	Write input. At the trailing edge of a low going input signal, control/data bytes are written.
24	RC5 (/D/C)	D/C	Control/Data input. When low, reads and writes will reference the data register. When high, reads and writes will reference the control register.
23	RC4 (/X/Y)	X/Y	Selects between the X axis and the Y axis. When low, the X axis is selected. When high, the Y axis is selected.
11	RE2 (/CS)	CS	This pin selects the encoder IC (enables it). When low, the IC is enabled. When high, the encoder IC is disconnected from PORT D.

Table 8. Interface connections from the QIC to the encoder IC.

4.1.1 ENCODER PROGRAMMING AND READING

For easier programming of the encoder interface, utility functions have been written to do all the necessary tasks of reading, writing and setting up the encoder IC. The two functions,

```
void init_encoder(void)
float read_encoder(int axis)
```

are specifically designed for this purpose. The functions are contained in **qic.h**. The user should include this file in their C source code in order to make use of the functions.

QIC CARRIER V1 MANUAL

The function `init_encoder()` should be called first to initialize the registers to zero and to setup the proper functions. After that, the function `read_encoder(axis)` should be called, where `axis` is either `X_AXIS`, or `Y_AXIS` as defined in the same header file.

The function will return a floating point value representing the number of counts that the encoder wheel has advanced. To calculate degrees from this count value, the count value should be divided by the appropriate scaling factor. Determination of this factor is as follows.

$$AngleDegrees = \frac{360}{(N \times 4)} \times EncoderCount$$

Where `N` is the encoder wheel resolution in counts per revolution,
the factor of 4 is for quadrature mode,
and the `EncoderCount` is the value read from the encoder using the
function `read_encoder(axis)`.

For further details on programming, the user is directed to the information in the following pages, or the included source code. Alternatively, the user may go directly to the US Digital web site to obtain additional programming information and generic examples written in C.

QIC CARRIER V1 MANUAL

4.1.2 ENCODER REGISTER ACCESS

<i>Chip Access</i>								
D7	D6	D5	C/D	RD	WR	X/Y	CS	Function
X	X	X	X	X	X	X	1	Disable chip
0	0	0	1	1	↓ ⁵	0	0	Write to XRLD
0	0	0	1	1	↓	1	0	Write to YRLD
1	0	0	1	1	↓	X	0	Write to both XRLD and YRLD
0	0	1	1	1	↓	0	0	Write to XCMR
0	0	1	1	1	↓	1	0	Write to YCMR
1	0	1	1	1	↓	X	0	Write to both XCMR and YCMR
0	1	0	1	1	↓	0	0	Write to XIOR
0	1	0	1	1	↓	1	0	Write to YIOR
1	1	0	1	1	↓	X	0	Write to both XIOR and YIOR
0	1	1	1	1	↓	0	0	Write to XIDR
0	1	1	1		↓	1	0	Write to YIDR
1	1	1	1	1	↓	X	0	Write to both XIDR and YIDR
X	X	X	0	1	↓	0	0	Write to X Preset register, increment address counter
X	X	X	0	1	↓	1	0	Write to Y Preset Register, increment address counter
X	X	X	0	↓	1	0	0	Read X Output latch, increment address counter
X	X	X	0	↓	1	1	0	Read Y Output latch, increment address counter
X	X	X	1	↓	1	0	0	Read Y FLAG register
X	X	X	1	↓	1	1	0	Read Y FLAG register

Table 9. Registers of the LS7266R1.

⁵ ↓ Indicates a low going signal, triggered on the falling edge.

QIC CARRIER V1 MANUAL

4.1.3 ENCODER PROGRAMMING INFORMATION

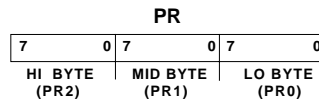
The Following Section is Reprinted from the LS7266R1 Documentation:

LS7266R1 Registers:

LS7266R1 has a set of registers associated with each X and Y axis. All X-axis registers have the name prefix X, whereas all Y-axis registers have the prefix Y. Selection of a specific register for Read/Write is made from the decode of the three most significant bits (D7-D5) of the data-bus. CS input enables the IC for Read/Write. C/D input selects between control and data information for Read/Write. Following is a complete list of LS7266R1 registers.

Preset Registers: XPR and YPR

Each of these PRs are 24-bit wide. 24-bit data can be written into a PR, one byte at a time, in a sequence of three data write cycles.



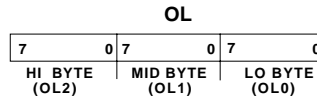
Counters: XCNTR and YCNTR

Each of these CNTRs are 24-bit synchronous Up/Down counters. The count clocks for each CNTR is derived from its associated A/B inputs. Each CNTR can be loaded with the content of its associated PR.

Output Latches: XOL and YOL

Each OL is 24-bits wide. In effect, the OLs are the output ports for the CNTRs. Data from each CNTR can be loaded into its associated OL and then read back on the data-bus, one byte at a time, in a sequence of three data Read cycles.

QIC CARRIER V1 MANUAL

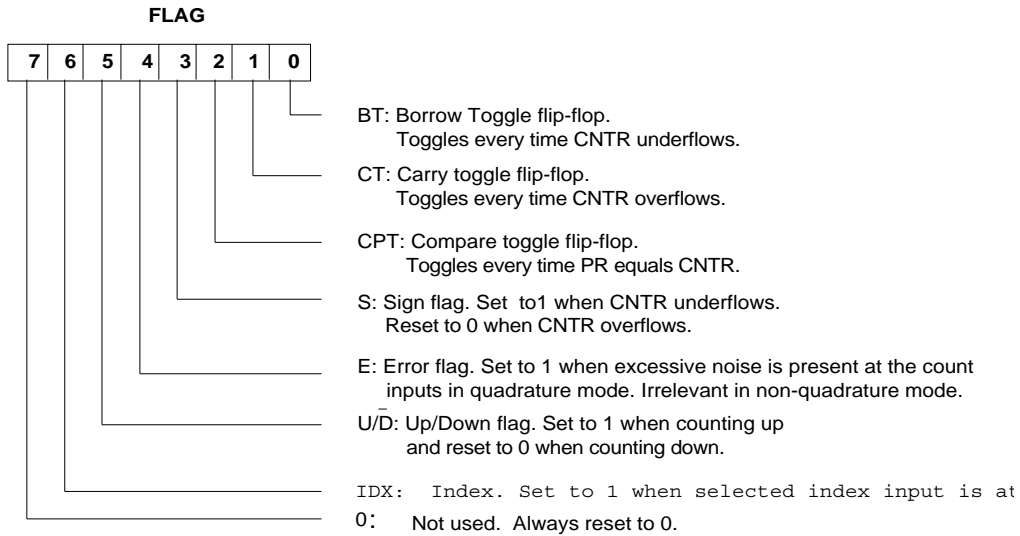


Byte Pointers: XBP and YBP

The Read and Write operations on an OL or a PR always accesses one byte at a time. The byte that is accessed is addressed by one of the BPs. At the end of every data Read or Write cycle on an OL or a PR, the associated BP is automatically incremented to address the next byte.

Flag Register: XFLAG and YFLAG

The FLAG registers hold the status information of the CNTRs and can be read out on the data bus. The E bit of a FLAG register is set to 1 when the noise pulses at the quadrature inputs are wide enough to be validated by the input filter circuits. E = 1 indicates excessive noise at the inputs but not a definite count error. Once set, E can only be reset via the RLD.



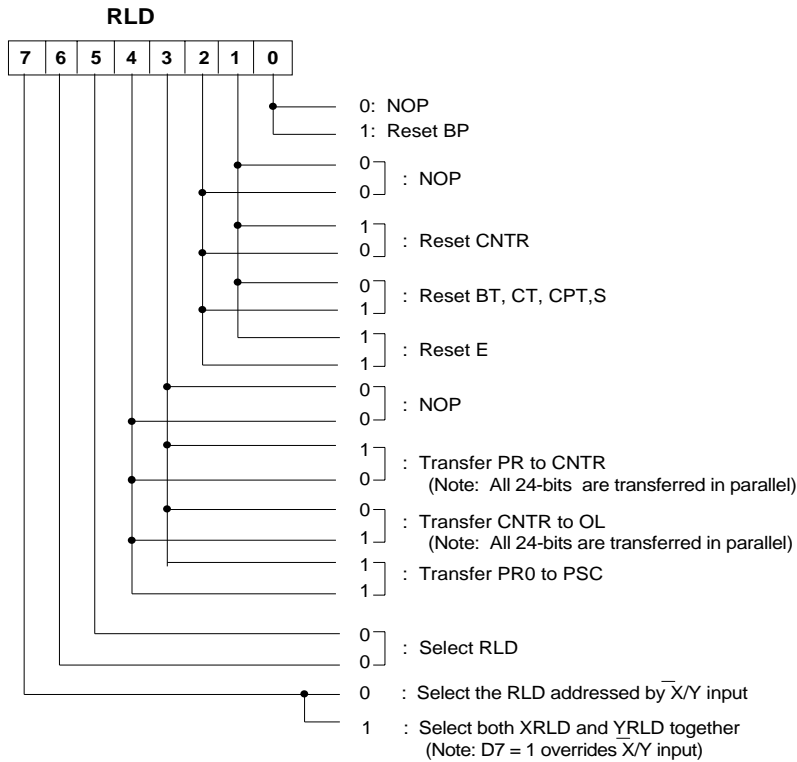
Filter Clock Prescalers: XPSC and YPSC

Each PSC is an 8-bit programmable modulo-N down counter, driven by the FCK clock. The factor N is down loaded into a PSC from the

QIC CARRIER V1 MANUAL

associated PR low byte register PR0. The PSCs provide the ability to generate independent filter clock frequencies for each channel. The PSCs generate the internal filter clock, FCKn used to validate inputs xA, xB, yA, yB in the quadrature mode.

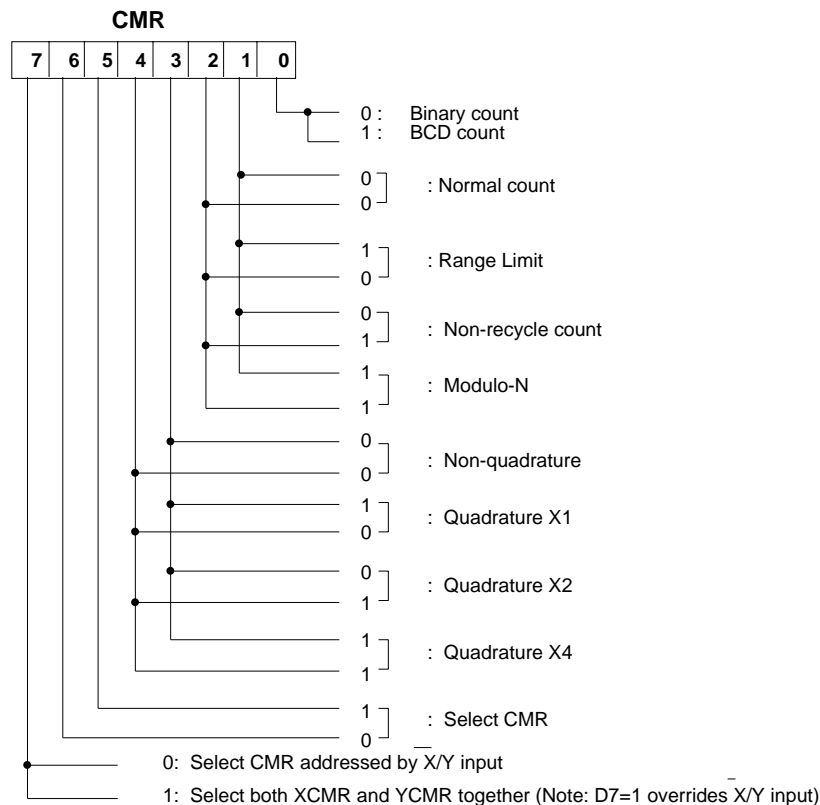
Final filter clock frequency $f_{FCKn} = (f_{CK}/(n+1))$, where $n = PSC = 0$ to F_{FH} . For proper counting in the quadrature mode, $f_{FCKn} \geq 8f_{QA}$ (or $8f_{QB}$), where f_{QA} and f_{QB} are the clock frequencies at inputs A and B. In non-quadrature mode filter clock is not needed and the FCK input (Pin 2), should be tied to V_{DD}



Counter Mode Registers: XCMR and YCMR

The CNTR operational mode is programmed by writing into the CMRs.

QIC CARRIER V1 MANUAL



DEFINITIONS OF COUNT MODES:

Range Limit. In range limit count mode, an upper and a lower limit is set, mimicking limit switches in the mechanical counterpart. The upper limit is set by the content of the PR and the lower limit is set to be 0. The CNTR freezes at CNTR=PR when counting up and at CNTR=0 when counting down. At either of these limits, the counting is resumed only when the count direction is reversed.

Non-Recycle. In non-recycle count mode, the CNTR is disabled, whenever a count overflow or underflow takes place. The end of cycle is marked by the generation of a Carry (in Up Count) or a Borrow (in Down Count). The CNTR is re-enabled when a reset or load operation is performed on the CNTR.

Modulo-N. In modulo-N count mode, a count boundary is set between 0 and the content of PR. When counting up, at CNTR=PR, the CNTR is

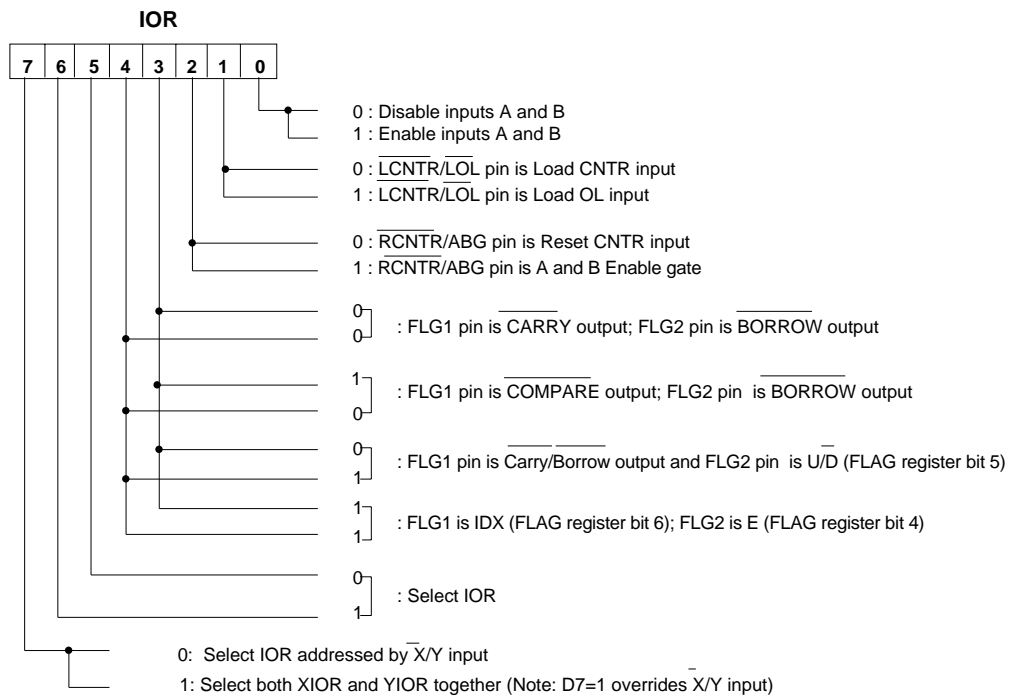
QIC CARRIER V1 MANUAL

reset to 0 and the up count is continued from that point. When counting down, at CNTR=0, the CNTR is loaded with the content of PR and down count is continued from that point.

The modulo-N is true bidirectional in that the divide-by-N output frequency is generated in both up and down direction of counting for same N and does not require the complement of N in the UP instance. In frequency divider application, the modulo-N output frequency can be obtained at either the Compare (FLG1) or the Borrow (FLG2) output. Modulo-N output frequency, $f_N = (f_i / (N + 1))$ where f_i = Input count frequency and $N=PR$.

Input/Output Control Register: XIOR and YIOR

The functional modes of the programmable input and output pins are written into the IORs.

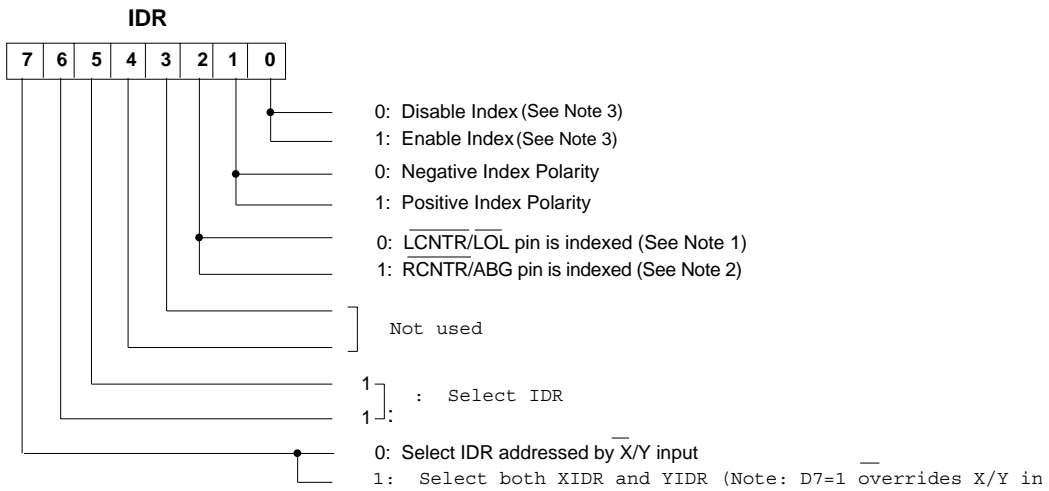


INDEX CONTROL REGISTERS: XIDR and YIDR

QIC CARRIER V1 MANUAL

Either the LCNTR/LOL or the RCNTR/ABG inputs can be initialized to operate as an index input. When initialized as such, the index signal from the encoder, applied to one of these inputs performs either the Reset CNTR or the Load CNTR or the Load OL operation synchronously with the quadrature clocks. Note that only one of these inputs can be selected as the Index input at a time and hence only one type of indexing function can be performed in any given set-up.

The index function must be disabled in non-quadrature count mode.



Note 1: Function selected for this pin via IOR, becomes the operating INDEX function.

Note 2: RCNTR/ABG input must also be initialized as the reset CNTR input via IOR

Note 3: "Enable Index" causes the synchronous mode for the selected index input (as described in Pin 18 and Pin 19 sections of the I/O Description) to be enabled. "Disable Index" causes the non-synchronous mode to be enabled. The input, however, is not disabled in either selection.

QIC CARRIER V1 MANUAL

5 MEDIUM CURRENT PERIPHERAL DRIVERS

The QIC Carrier Board is equipped with a 4 channel, medium current driver. This device is capable of continuously sinking / sourcing up to 500mA of current at voltages up to 18 volts. With a peak current output of 1.2A (each channel), the peripheral drivers are ideal for driving small DC motors, or small stepper motors.

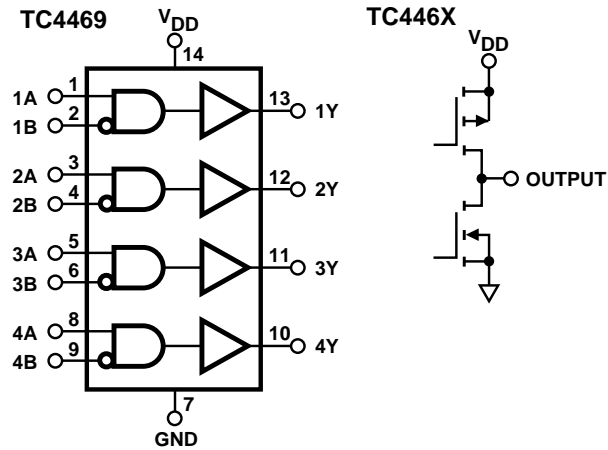


Figure 12. Peripheral driver details.

The 'B' inputs are grounded to allow the outputs to be driven by the 'A' inputs alone. The 'A' inputs are connected to PORT C of the QIC Processor Core (RC0 – RC3). Table 10 shows the connection details.

<i>Peripheral Driver Connection Details</i>				
<i>QIC</i>				
<i>Pin</i>	<i>Name</i>	<i>Function</i>	<i>Channel</i>	<i>J13 Pin</i>
21	RC2	M0 PWM (PWM1)	Y1	1
19	RC0	DIR 0	Y2	2
20	RC1	M1 PWM (PWM2)	Y3	3
22	RC3	DIR 1	Y4	4

Table 10. Peripheral driver connection details.

QIC CARRIER V1 MANUAL

5.1 PERIPHERAL DRIVER CONFIGURATIONS

The configuration of the drivers is designed to allow bi-directional driving of motors, driving of stepper motors, as well as driving relays or similar loads. Note that **JP3** and **JP4** must be installed in the **2-3** position to enable PWM signals to pass to the drivers. In positions 1-2, the PWM signals are sent to the D/A output filters.

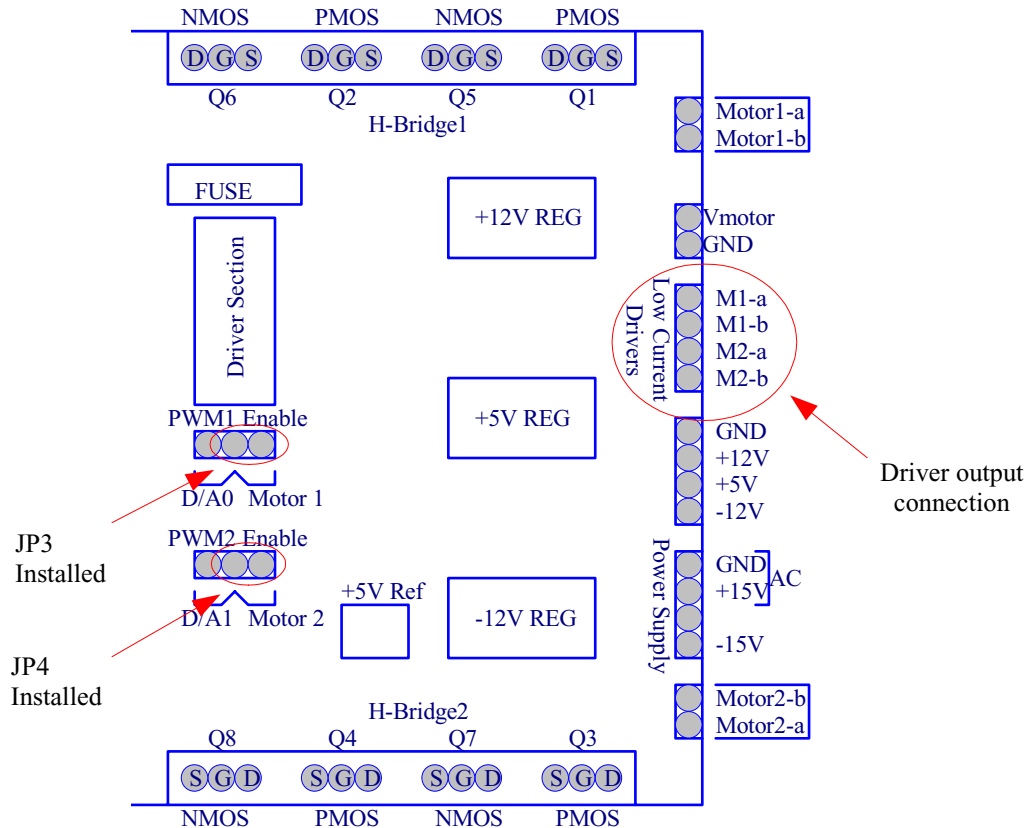


Figure 13. Setup of the jumpers and the location of peripheral outputs.

5.1.1 SOLENOID DRIVER CONFIGURATION

The peripheral drivers can be used to drive loads directly. Simply connect the load to the pin. Be certain not to exceed the device limits. In the case of inductive loads, the load

QIC CARRIER V1 MANUAL

should have a diode placed in reverse across it to prevent inductive spikes from damaging the driver. Although the device has built in protection for this, large inductive loads may temporarily exceed the 500mA inductive kickback rating for the device. Exceeding this rating may cause permanent damage to the device.

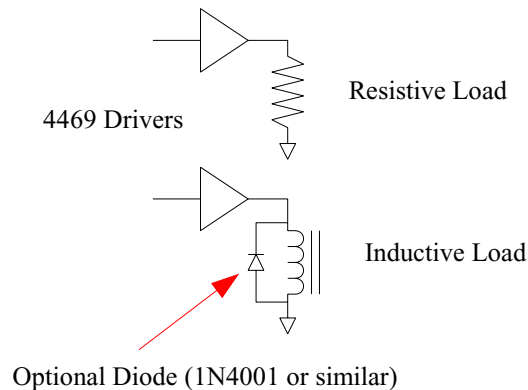


Figure 14. Driving resistive and inductive loads.

5.1.2 BI-DIRECTIONAL DC MOTOR DRIVER CONFIGURATION

The peripheral driver is capable of driving small DC motors in an H-bridge configuration. In this configuration, two channels are required to drive each motor in the forward and reverse directions. One of the channels (RC1 or RC2), controls the PWM speed signal to the driver. The other channel (RC0 or RC3) controls the direction. See Table 10 for the connection details on this. The speed is set by the PWM register value in software. See the included program examples for details on this.

QIC CARRIER V1 MANUAL

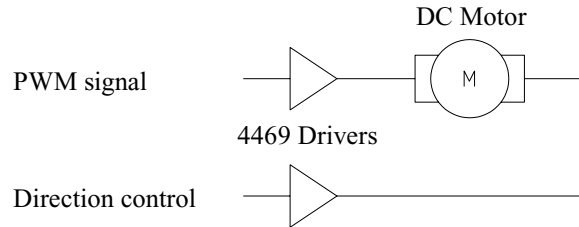


Figure 15. Connections for driving a small DC motor.

5.1.3 STEPPER MOTOR CONFIGURATION

The peripheral driver is capable of driving small stepper motors as well. In this configuration, 1 stepper motor can be driven directly from the outputs of the driver. The proper bit sequence will have to be written to PORT C to drive the stepper motor in the desired direction. Using this configuration, both full-stepping and micro-stepping is possible. The on board PWM is not used in this case. The included source code examples have details on driving the stepper motor in software.

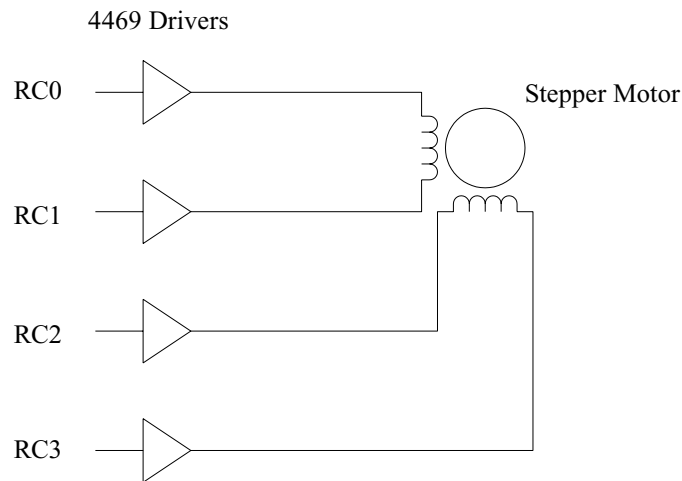


Figure 16. Details for driving a stepper motor.

6 HIGH CURRENT PERIPHERAL DRIVERS

The QIC Carrier Board is equipped with the option of installing MOSFETS to allow the driving of higher current loads. The inputs to the MOSFETS are driven from the outputs of the peripheral driver, so only one option is available at a time. The high current peripheral drivers are intended to be used in H-Bridge (full or half) configurations. The peripheral driver and the H-Bridge drivers may be used in any combination. That is, the user may choose to use only one channel to drive an H-bridge (half bridge configuration) section, or may select two channels (full bridge configuration).

The configuration of the drivers is designed to allow bi-directional driving of motors, driving of stepper motors, as well as driving relays or similar loads. Note that **JP3** and **JP4** must be installed in the **2-3** position to enable PWM signals to pass to the drivers. In positions 1-2, the PWM signals are sent to the D/A output filters. Figure 17 shows details on this.

In addition, power for the drivers must be supplied to the connections Vmotor and GND (J16). This can be the same power supply used by the rest of your circuit if the supply has sufficient capacity. Alternatively, this can be dedicated supply that powers just the high current drivers.

QIC CARRIER V1 MANUAL

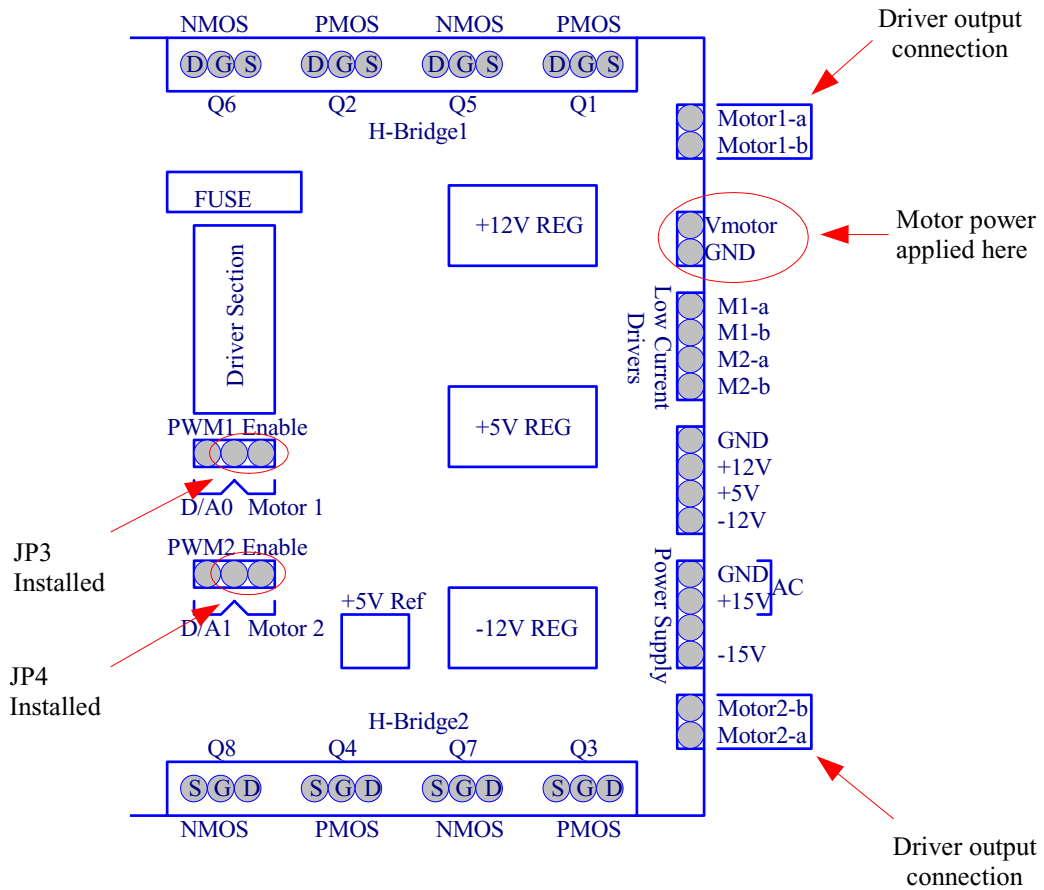


Figure 17. Setup and connections for the high current drivers

QIC CARRIER V1 MANUAL

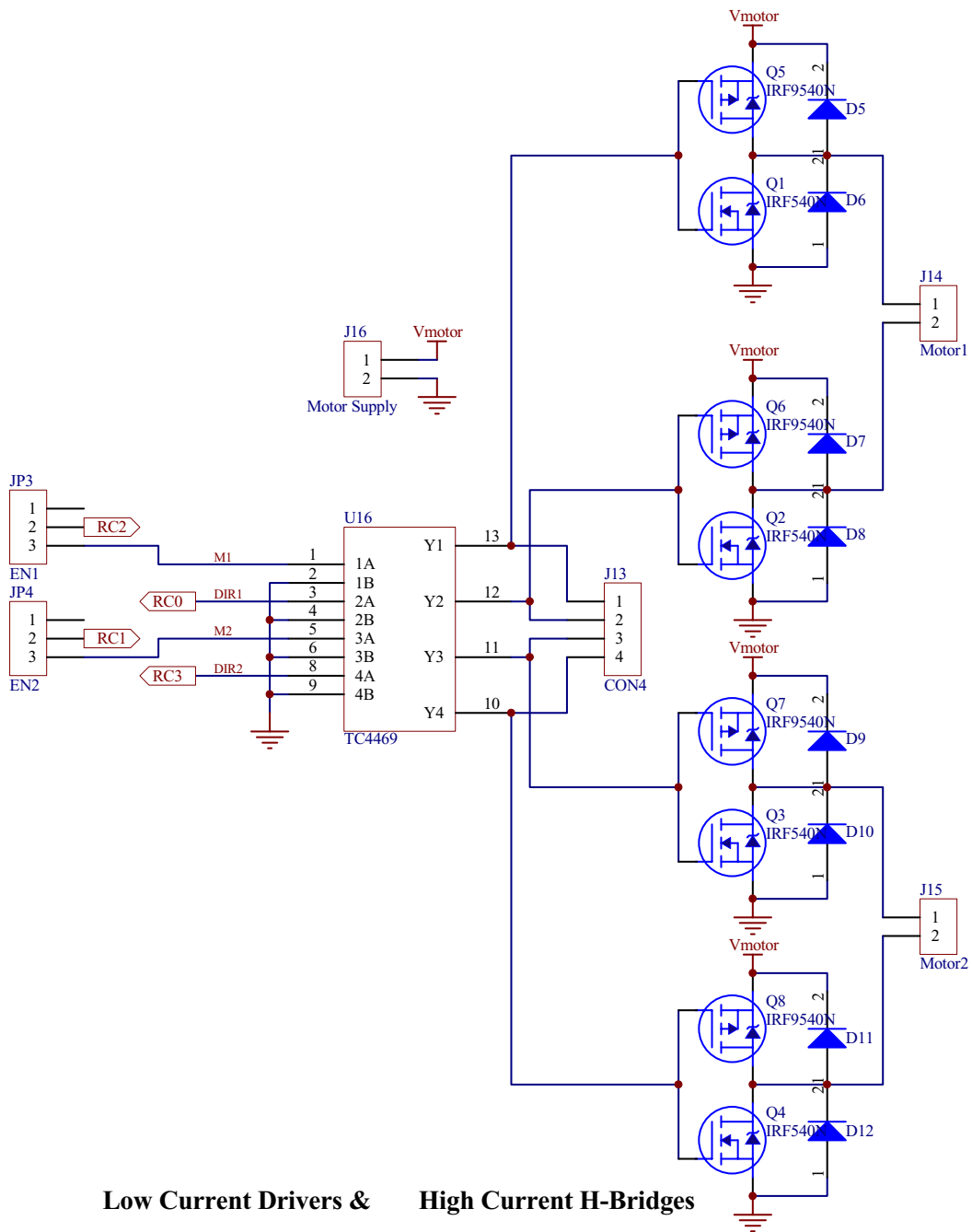


Figure 18. Detailed schematic of the high current drivers.

QIC CARRIER V1 MANUAL

6.1 INSTALLATION OF MOSFETS

Figure 19 shows the details of installing the MOSFETS in their appropriate places on the board. Recommended MOSFETS are the IRF9540N and IRF540N. Similar devices may be used to suit the user's application. Care should be taken not to exceed the design limitations of the circuit board. Currents less than 3A and voltages less than 25V should be used. Exceeding these limitations may cause damage to the traces on the circuit board.

Diodes should also be placed in the locations marked on the board. The diodes are intended to protect the MOSFETS from inductive turn-off spikes. Suitable general-purpose diodes are 1N4002 or similar. Specialized diodes may be selected to better suit the end application. When installing diodes, care must be taken to observe the polarity.

6.2 HIGH CURRENT DRIVER USAGE

Loads may be driven from the high current outputs in the same manner as from the medium current outputs. The added benefit is that there is more power available to the user. The section titled, "Medium Current Peripheral Drivers" should be read and understood before attempting to use the high current drivers.

QIC CARRIER V1 MANUAL

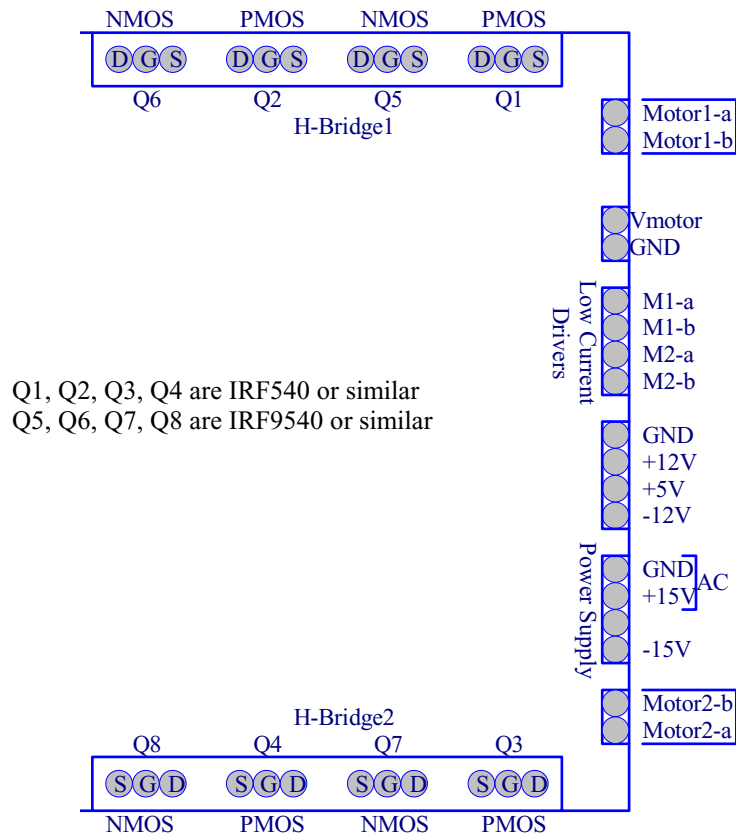


Figure 19. Installation of the MOSFETS for the high-current drivers.

6.2.1 HALF BRIDGE (SINGLE ENDED) USAGE

In the half bridge configuration, up to four loads may be independently driven. When driving loads in the half-bridge configuration, the output should be taken from the motor connectors, J14, and J15. The outputs will be available on pins 1 or 2 of the connector and is referenced to ground. Loads attached to the outputs must not exceed the current rating of the installed MOSFETS. For detailed examples, see the section titled “Solenoid Driver Configuration” for connection examples and details.

QIC CARRIER V1 MANUAL

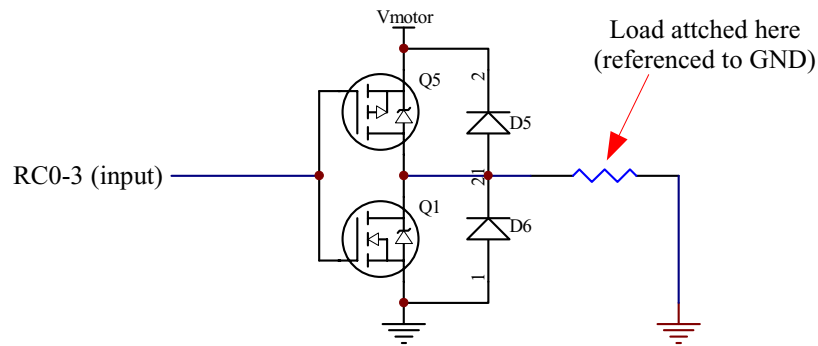


Figure 20. Single ended output driver connection.

6.2.2 FULL BRIDGE USAGE

In the full bridge mode, the drivers are capable of driving two DC motors, or one stepper motor.

To drive a DC motor, the power leads of the motor should be connected to J14 (or J15), pins 1 and 2. The motor is able to change directions by reversing the current flow through the motor, by turning on the appropriate section of the H-bridge. Detailed descriptions of how H-Bridges function may be found in many texts covering basic electronics. For software examples, see the included code for reference.

QIC CARRIER V1 MANUAL

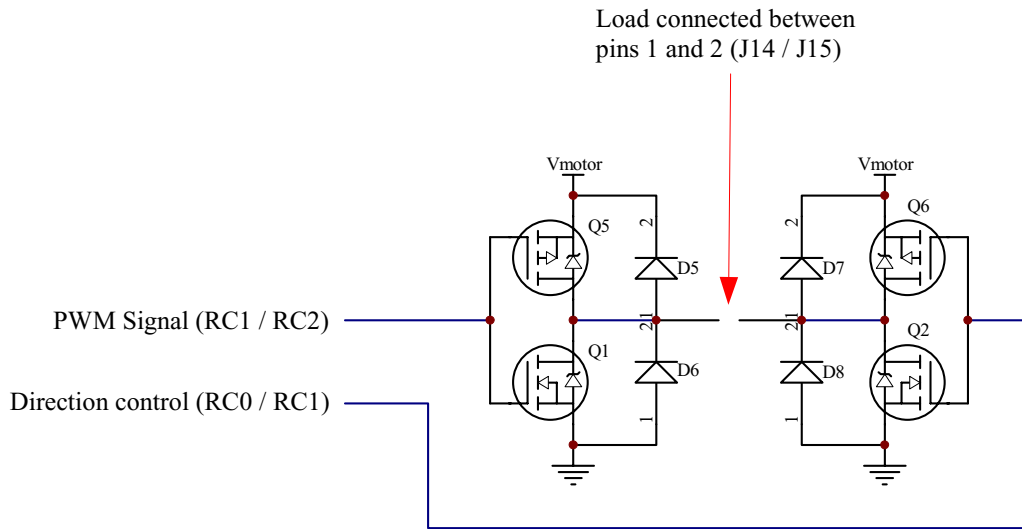


Figure 21. Full bridge connection of high current output drivers.